AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1-18. (*Canceled)*

19. (*Previously presented*) A bus architecture, comprising:

first, second, and third bus portions;

a first switch configured to enable/disable a connection between the first and second bus portions; and

a second switch configured to enable/disable a connection between the second and third bus portions,

wherein each of the first, second, and third bus portion operate based on a bus start signal and a data complete signal such that data transfer on the bus starts when the bus start signal is enabled and the data complete signal is disabled,

wherein a delay between enabling of the bus start signal and disabling of the data complete signal varies based on enabled/disabled states of the first and second switches.

20. (*Previously presented*) The bus architecture of claim 19, wherein the variance in the delay between the enabling of the bus start signal and the disabling of the data complete signal is based on a common bus signal.

21. (*Previously presented*) The bus architecture of claim 20, wherein the variance in the delay between the enabling of the bus start signal and the disabling of the data complete signal is accomplished by varying a number of clock signals to wait.

22. (*Previously presented*) The bus architecture of claim 20, wherein the variance in the delay between the enabling of the bus start signal and the disabling of the data complete signal is accomplished by varying a period of the clock signal.

23. (*Previously presented*) The bus architecture of claim 19,

wherein the delay is a first delay when both first and second switches are disabled, the delay is a second delay when first switch is enabled and second switch is disabled, and the delay is a third delay when both switches are enabled, and

wherein the first delay is shorter than the second delay and the second delay is shorter than the third delay.